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OIPE JC87
SEP 12 2002
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Lifeng Wu et al.		
Assignee:	Celestry Design Technologies, Inc.		
Title:	Hot-Carrier Circuit Reliability Simulation		
Serial No.:	09/832,933	Filing Date:	April 11, 2001
Examiner:	Unknown	Group Art Unit:	2123
Docket No.:	M-10096 US	Conf. No.:	5253

San Francisco, California
September 12, 2002

Attn: Office of Petitions
Box DAC
Commissioner for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;

2. a representation that a search has been made, other than as described above; or

3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

EXPRESS MAIL LABEL NO:
EL873331053US

Respectfully submitted,

Michael G. Cleveland
Reg. No. 46,030

LAW OFFICES OF
SKJERVEN MORRILL LLP
3 EMBARCADERO CENTER
SUITE 2800
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Application No.
	M-10096 US	09/832,933
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Lifeng Wu et al.	
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	April 11, 2001	2123

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U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,533,197	Jul. 2, 1996	Moran et al.			
	AB	5,600,578	Feb. 4, 1997	Fang et al.			
	AC	5,606,518	Feb. 25, 1997	Fang et al.			
	AD	5,634,001	May 27, 1997	Mittl et al.			
	AE	5,974,247	Oct. 26, 1999	Yonezawa			
	AF	6,024,478	Feb. 15, 2000	Yamamoto			
	AG	6,047,247	Apr. 4, 2000	Iwanishi et al.			
	AH	6,278,964	Aug. 21, 2001	Fang et al.			

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AI ✓	Karam, Medhat, et al., "Implmentation of Hot-Carrier Reliability Simulation in Eldo" and related Internet material, Deep Submicron Technical Publication, dated September 2000.
	AJ ✓	Lou, Choon-Leong, et al., "A Novel Single-Device DC Method for Extraction of the Effective Mobility and Source-Drain Resistances of Fresh and Hot-Carrier Degraded Drain-Engineered MOSFET's", IEEE Transactions on Electron Devices, Vol. 45, No. 6, June 1998, pp. 1317-1323.
	AK ✓	Wong, H., et al., "Simulation of Hot-Carrier Reliability in MOS Integrated Circuits", PROC. 21st International Conference on Microelectronics, Vol. 2, NIS, Yugoslavia, September 14-17, 1997, pp. 625-628.
	AL ✓	Hwang, Nam, et al., "Hot-Carrier Induced Series Resistance Enhancement Model (HISREM) of nMOSFET'S for Circuit Simulations and Reliability Projections", Microelectronics and Reliability, Vol. 35, No. 2, pp. 225-239, February 1995, pp. 225-239.
	AM ✓	Aur, S., et al., "Modeling of Hot Carrier Effects for LDD Mosfets", 1985 Symposium of VLSI Technology, pp. 112-113.
	AN ✓	Jiang, Wenjie, et al., "Key Hot-Carrier Degradation Model Calibration and Verification Issues for Accurate AC Circuit-Level Reliability Simulation", IEEE, 1997, pp. 300-306.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AO	Hu, Chenming, "IC Reliability Simulation", IEEE Journal of Solid-State Circuits, Vol. 27, No. 3, March 1992, pp. 241-246.
	AP	Jiang, Wenjie, et al., "Assessing Circuit-Level Hot-Carrier Reliability", IEEE, 1998, pp. 173-179.
	AQ	Ling, C.H., et al., "Simulation of Logarithmic Time Dependence of Hot Carrier Degradation in PMOSFETs", Semicond. Sci. Technol. 10, 1995, pp. 1659-1666.
	AR	Li, Chester C., et al., "A New Bi-directional PMOSFET Hot-Carrier Degradation Model for Circuit Reliability Simulation", IEEE, 1992, pp. 20.7.1-20.7.4.
	AS	Quader, Khandker N., et al., "A Bidirectional NMOSFET Current Reduction Model for Simulation of Hot-Carrier-Induced Circuit Degradation", IEEE Transactions on Electron Devices, Vol. 40, No. 12, December 1993, pp. 2245-2254.
	AT	Leblebici, Y., et al., "An Integrated Hot-Carrier Degradation Simulator for VLSI Reliability Analysis", IEEE, 1990, pp. 400-403.
	AU	Hsu, Wen-Jay, et al., "Advanced Integrated-Circuit Reliability Simulation Including Dynamic Stress Effects, IEEE Journal of Solid-State Circuits, Vol. 27, No. 3, March 1992, pp. 247-257.
	AV	Chang, Steve S., et al., "A New MOSFET Hot Carrier Model in SPICE Feasible for VLSI Reliability Anaylsis", International Symposium on VLSI Technology, Systems, and Applications, Taipei, Taiwan, R.O.C., May 22-24, 1991, pp. 283-287.

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